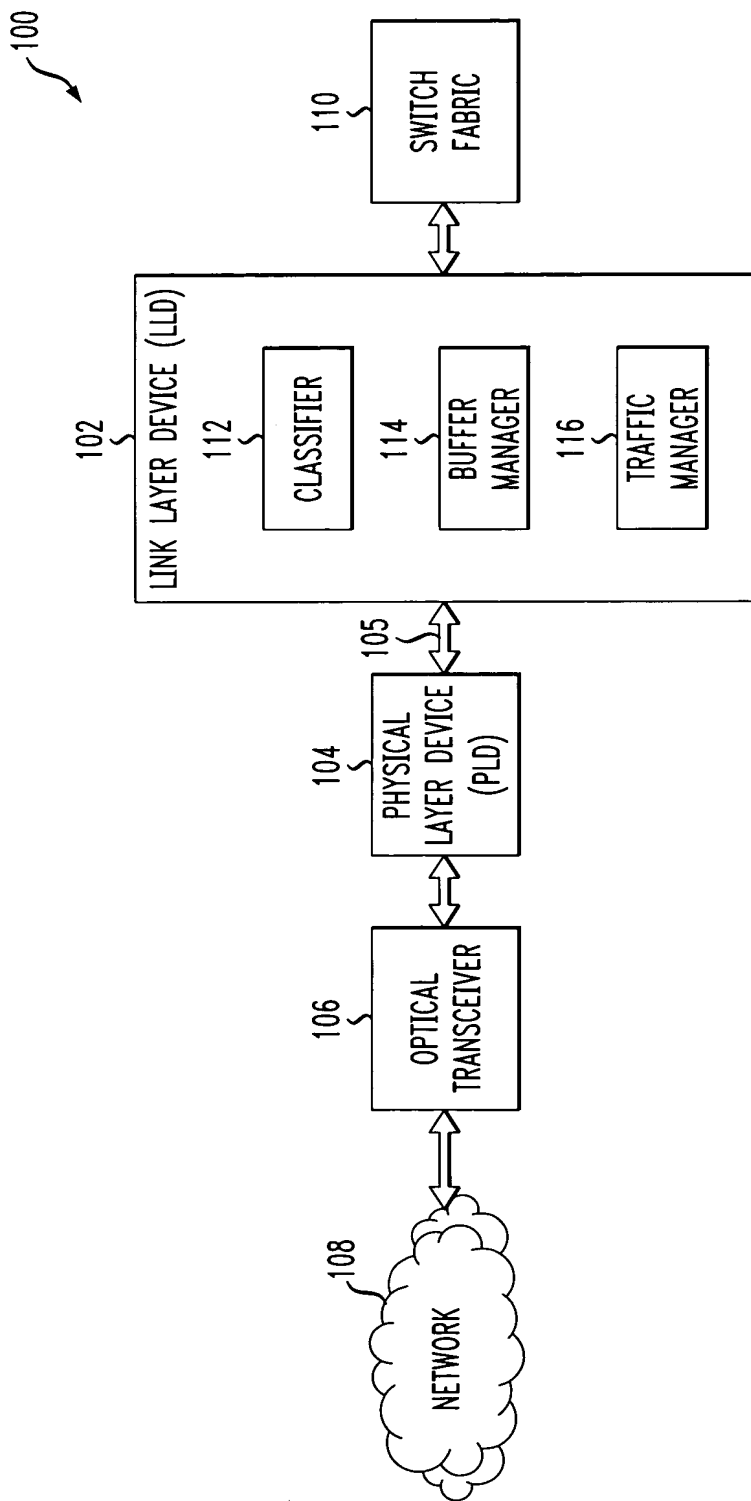




FIG. 1



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FIG. 2

F	A	C	I	FCS	F
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<u>FIELD NAME</u>	<u>SIZE (BITS)</u>
FLAG FIELD (F)	8 BITS
ADDRESS FIELD (A)	8 BITS
CONTROL FIELD (C)	8 OR 16 BITS
INFORMATION FIELD (I)	VARIABLE
FRAME CHECK SEQUENCE (FCS)	16 OR 32 BITS

FIG. 3

	PACKET OVERHEAD (ASSUMING MAX SIZE FOH = 8B)			
	FOH	SOH	PS	% OH
NO STUFFING, MIN SIZED PACKET	8	0	40	20%
MAX STUFFING, MIN SIZED PACKET	8	8	40	40%
NO STUFFING, MAX SIZED PACKET	8	0	9600	0.08%
MAX STUFFING, MAX SIZED PACKET	8	1920	9600	20%

ASSUMPTIONS:

- a) PACKET SIZE (PS):
40 - 9600 BYTES
- b) WORST-CASE HDLC BIT STUFFING OVERHEAD (SOH)
20% OF (a) = 8 - 1920 BYTES
- c) HDLC FRAME OVERHEAD (FOH)
5 - 8 BYTES

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FIG. 4

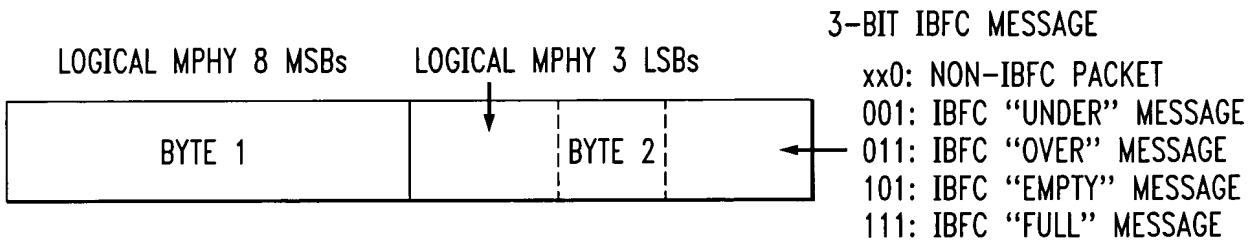
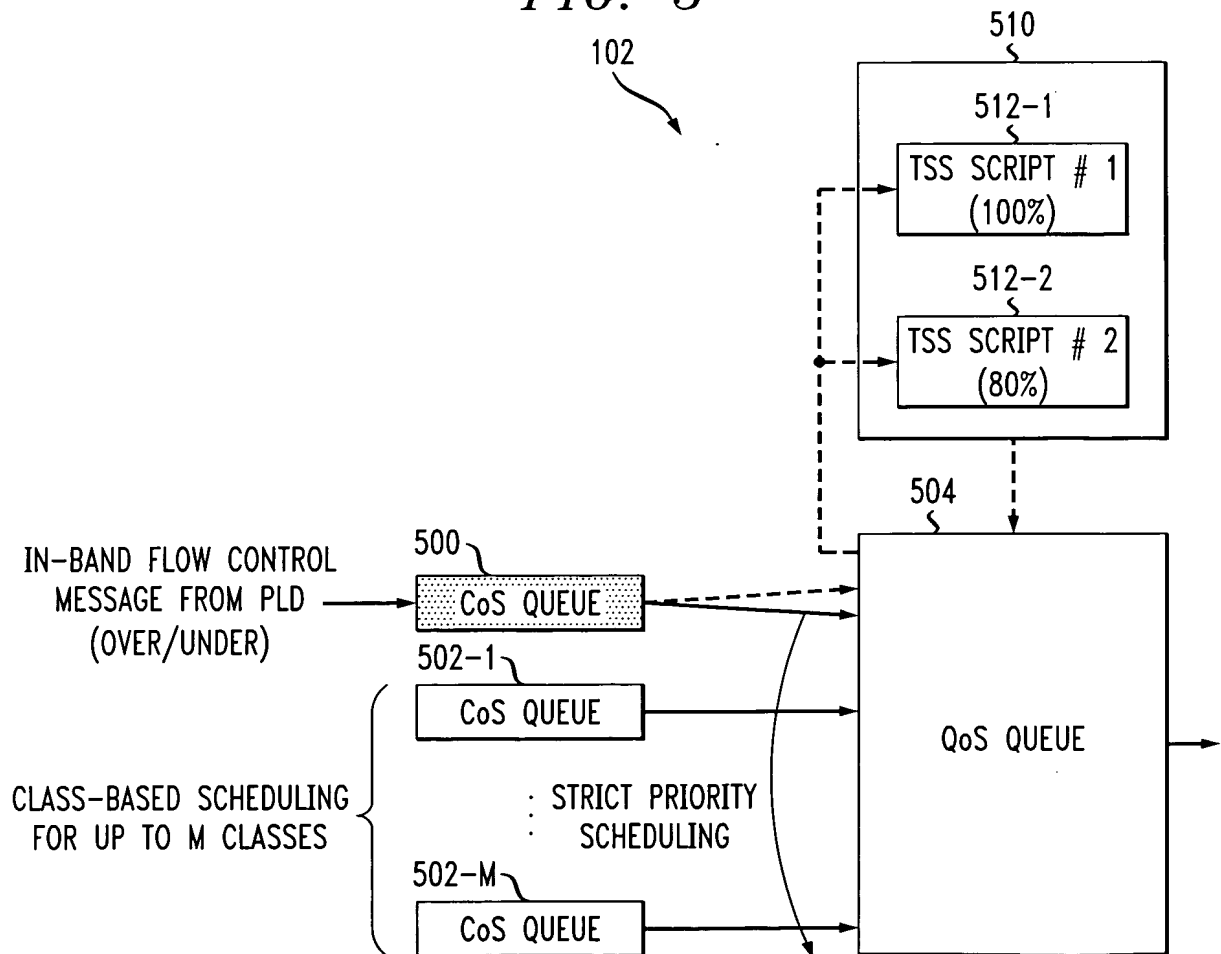


FIG. 5



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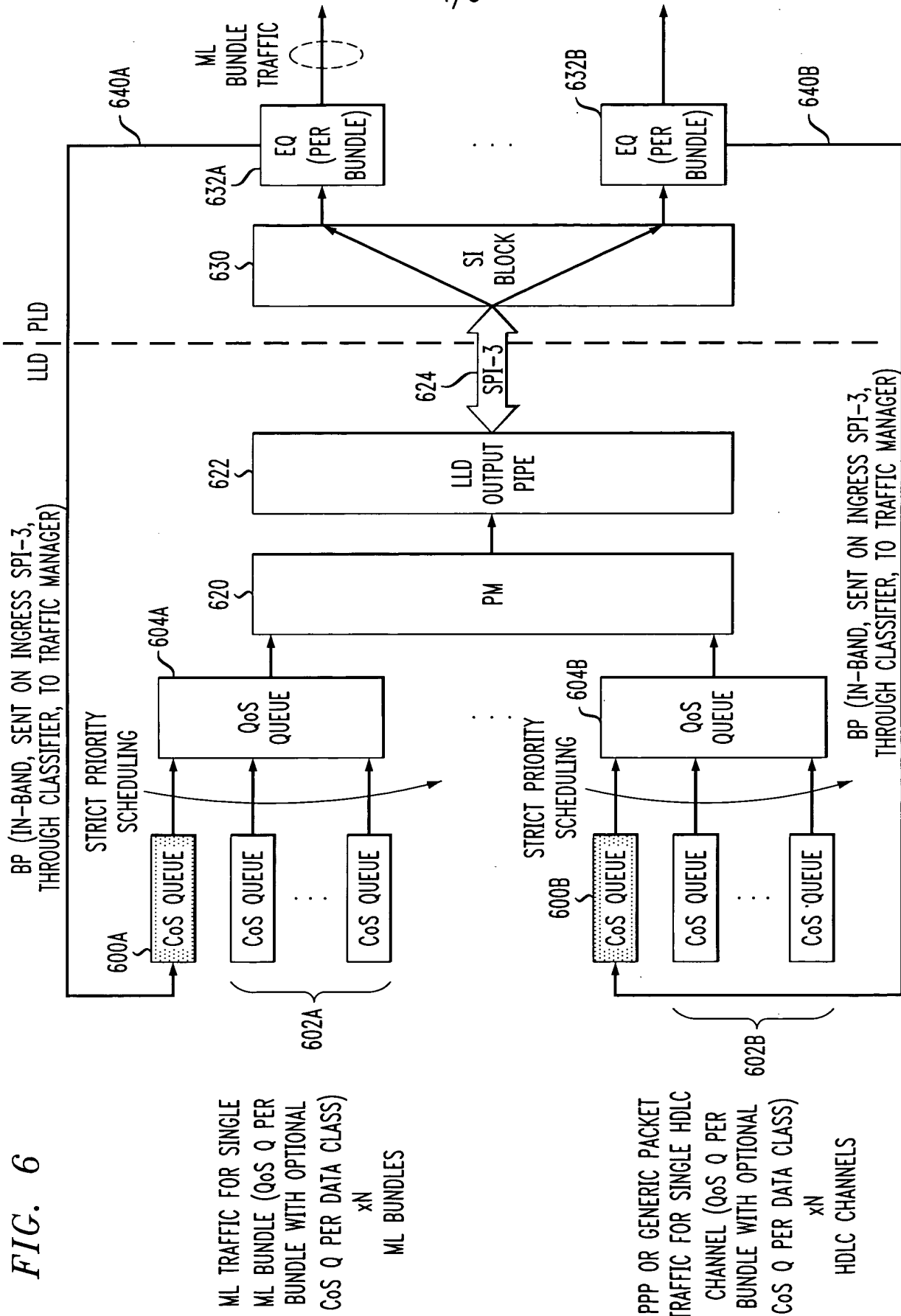
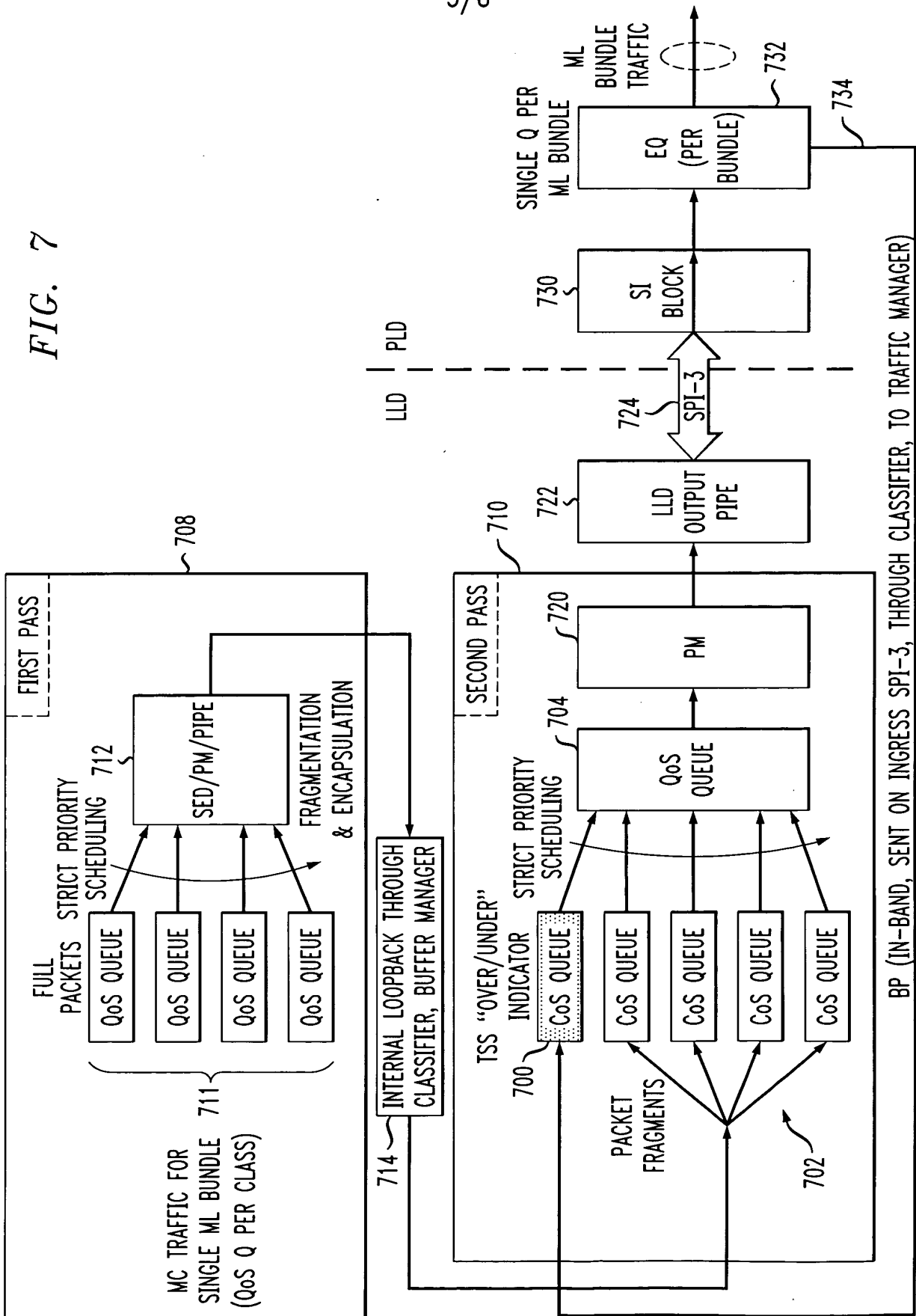


FIG. 6

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FIG. 7



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FIG. 8

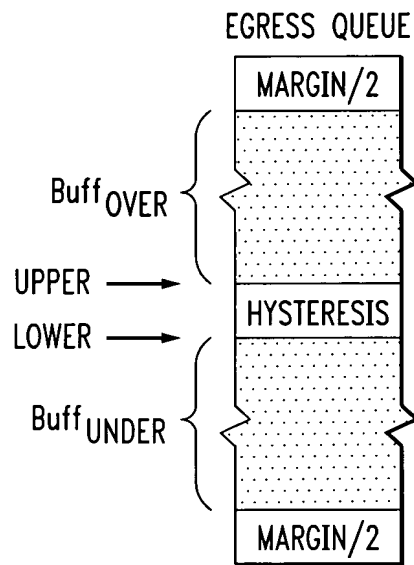


FIG. 9

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PARAMETER DEFINITIONS	
R_{PORT} : NOMINAL DATA RATE OF A PLD HDLC CHANNEL CORRESPONDING TO AN EQ.	D_{MTU} : DELAY DUE TO TRANSMISSION OF AN MTU-SIZED PACKET FROM LLD CoS QUEUE.
R_{FILL} : DATA INPUT (ENQUEUE) RATE OF PLD EQ.	D_{LLD} : WORST-CASE CLASSIFICATION DELAY OF LLD.
R_{DRAIN} : DATA OUTPUT (DEQUEUE) RATE OF PLD EQ.	D_{PIPE} : OUTPUT PIPELINE DELAY OF LLD.
FCL : FLOW CONTROL LATENCY.	D_{PLD} : PLD DELAY IN TRANSMITTING IBFC MESSAGE.
$Buff = R_{FILL} - R_{DRAIN} * FCL$ $ R_{FILL} - R_{DRAIN} = R_{PORT} - 0.8 R_{PORT} = 0.2 * R_{PORT}^{\dagger}$ $FCL = D_{MTU} + D_{LLD} + D_{PIPE} + D_{PLD}^{\ddagger}$	
<p>USE THE FOLLOWING FACTS AND WORST-CASE ASSUMPTIONS:</p> $D_{MTU-L} = MTU \div (0.8 * R_{PORT}); D_{MTU-U} = MTU \div R_{PORT}$ $D_{LLD} \leq 20 \mu\text{sec.}^{\dagger\dagger}$ $D_{PIPE} \leq 6 \mu\text{sec.}^{\ddagger\dagger}$ $D_{PLD} \leq 1 \mu\text{sec.}^{\S}$	
$Buff_{UNDER} = (0.2 * R_{PORT}) * ([MTU/(0.8 * R_{PORT})] + 20 \mu\text{s} + 6 \mu\text{s} + 1 \mu\text{s})$ $= (0.2 * R_{PORT}) * ([MTU/(0.8 * R_{PORT})] + 27 \mu\text{s})$ $= R_{PORT} * ([0.25 * MTU/R_{PORT}] + 5.4 \mu\text{s})$ $= (0.25 * MTU) + (R_{PORT} * 5.4 \mu\text{s})$	
$Buff_{OVER} = (0.2 * R_{PORT}) * ([MTU/R_{PORT}] + 20 \mu\text{s} + 6 \mu\text{s} + 1 \mu\text{s})$ $= (0.2 * R_{PORT}) * ([MTU/R_{PORT}] + 27 \mu\text{s})$ $= R_{PORT} * ([0.2 * MTU/R_{PORT}] + 6.75 \mu\text{s})$ $= (0.2 * MTU) + (R_{PORT} * 6.75 \mu\text{s})$	

[†] HDLC R_{DRAIN} IS AT MOST 20% GREATER OR LESS THAN SCHEDULER R_{FILL}

[‡] FCL IS EQUAL TO THE SUM OF THE DELAYS (D) SHOWN

^{††} W.C. DELAY OF THE FLOW CONTROL MESSAGE THROUGH CLASSIFICATION TO THE TRAFFIC SHAPER

^{‡‡} LLD OUTPUT PIPELINE DELAY

[§] W.C. DELAY FROM FLOW CONTROL MESSAGE GENERATION IN PLD TO TRANSMISSION ON THE SPI-3 INGRESS INTERFACE

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FIG. 10

HDLC CHANNEL SIZE	HDLC CHANNEL RATE (IN Kbps)	MTU (IN BYTES)	Buff UNDER (IN BYTES)	Buff OVER (IN BYTES)	LOWER BOUND EQ SIZE (IN BYTES)	WORST-CASE EQ SIZE (IN BYTES)
DS0	64	576	145	116	261	586
	64	1518	380	304	684	1432
	64	9600	2401	1921	4322	8708
DS1	1544	576	146	117	263	590
	1544	1518	381	305	686	1436
	1544	9600	2402	1922	4324	8712
8 x DS1	12352	576	153	126	279	622
	12352	1518	388	315	703	1470
	12352	9600	2409	1931	4340	8744